10/007,833

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,122 B2
DATED : September 14, 2004
INVENTOR(S) : Leslie R. Avery et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings,
Figure 1A, please change reference numeral "125" to -- 129 --.
Figure 1B, please change reference numerals "125", "241" and "242" to -- 129 --, -- 141 -- and -- 142 --, respectively.
Figure 2(A)-(D), please add reference numeral -- 136 -- at the first gate of transistor T1.

Column 11,
Line 30, please change "^{318}A" to -- 318_{A} --.

Column 16,
Line 56, please change "arid" to -- and --.
Line 67, please change "translstor" to -- transistor --.

Column 17 ,
Line 3, please change "lowing" to -- forming --.
Line 12, please change "firs'" to -- first --.
Line 13, please change "0.8 to 0.8" to -- 0.6 to 0.8 --.
Line 16, please change "typo" to -- type --.
Line 18, please change "ESO" to -- ESD --.
Line 34, please change "In" to -- in --.
Line 35, please change "N-wall, at least two cascaded" to -- N-well, at least two cascoded --.
Line 63, please change "pad end" to -- pad and --.
Line 65, please change "ESO" to -- ESD --.

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DATED : September 14, 2004
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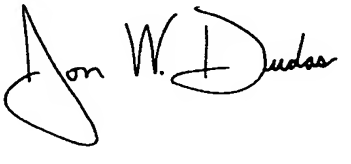
Column 18,
Line 11, please change "MOS PET" to -- MOSFET --.
Line 22, please change "In" to -- in --.
Line 33, please change "P-will" to -- P-well --.
Line 33, please change "In" to -- in --.

Signed and Sealed this

Seventeenth Day of May, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office